ASTERICS – CLEOPATRA
DELIVERABLE D5.4

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With many thanks to Mattia Rizzi (Cern) and Lex van der Gracht (VU)

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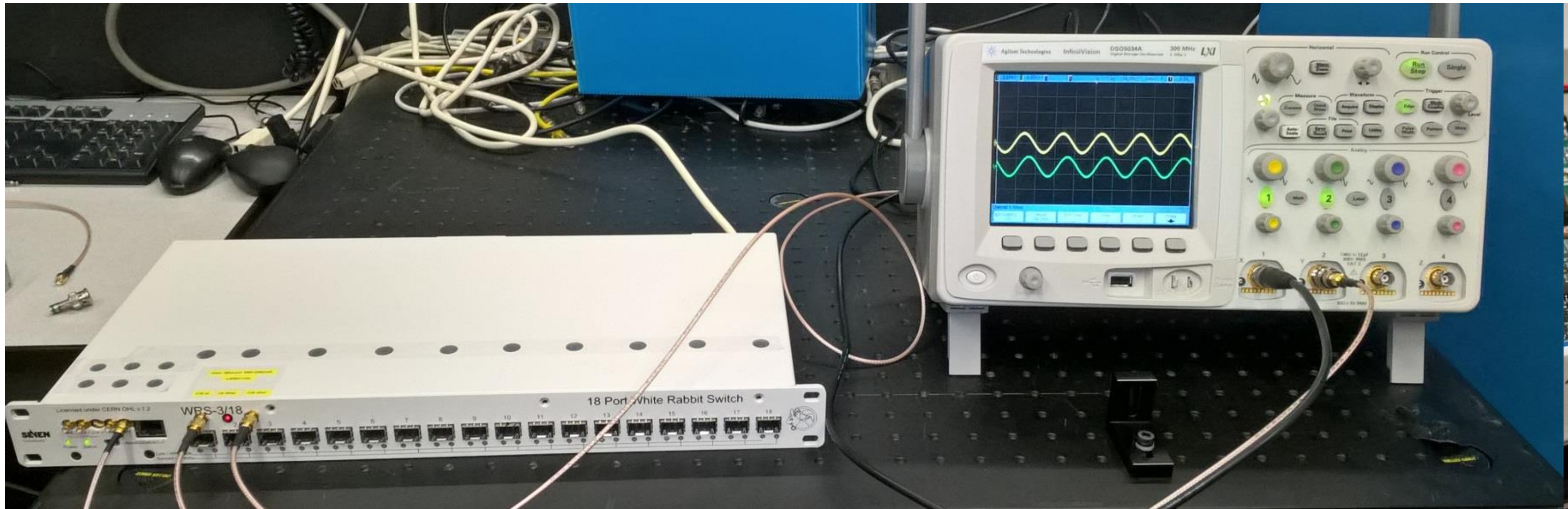


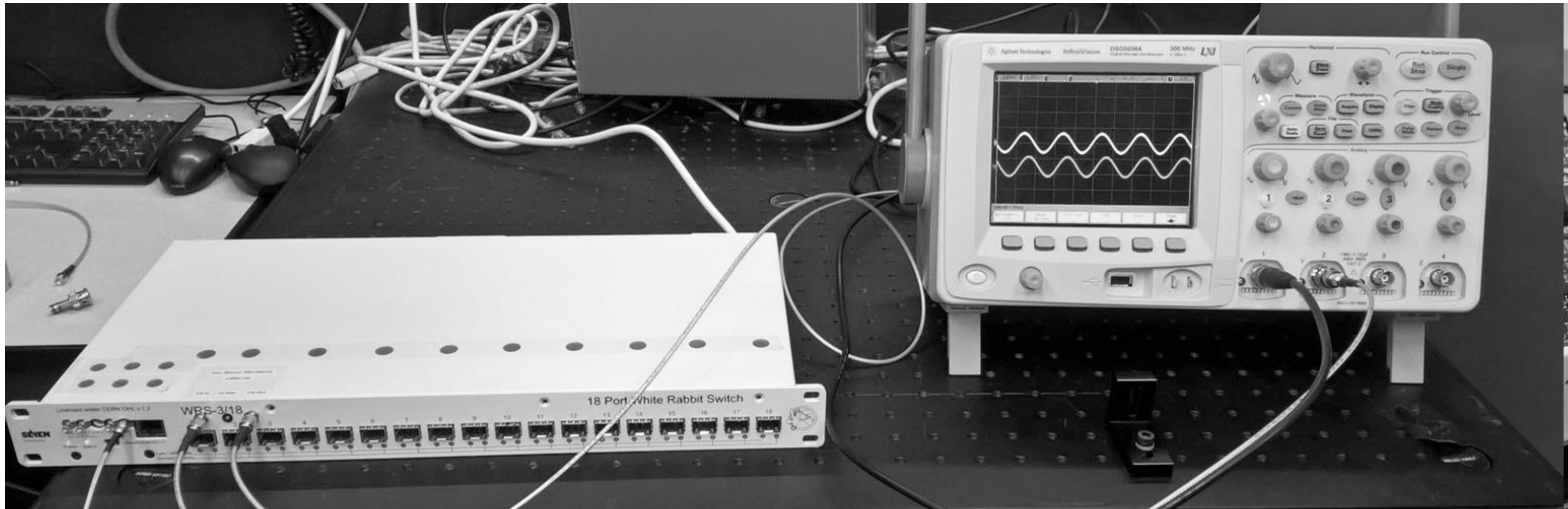
D5.4 Hardware for maser-level time & frequency distribution in public networks

Deliverables:

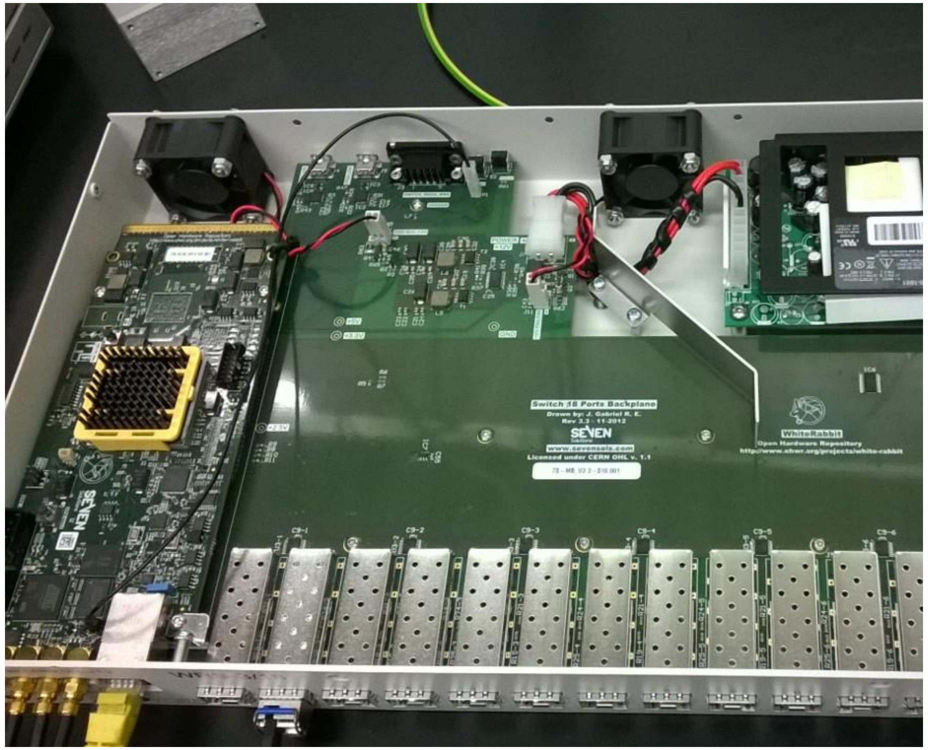
#1. Improve stability White Rabbit (WR) switches: either employ 'home-made' modifications (ongoing work), or buy 7S product (budget available, but products not yet).

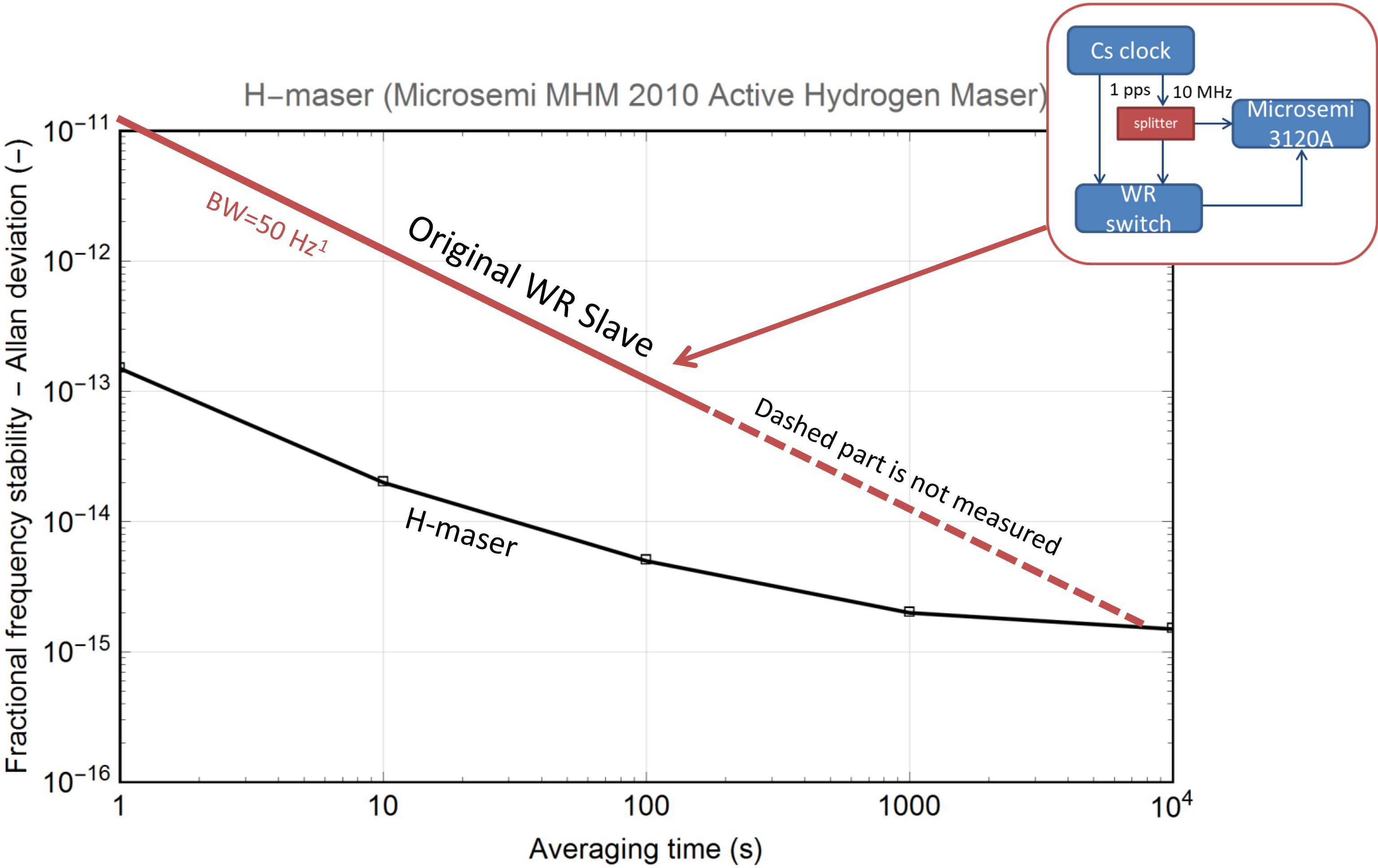
#2. Share experience obtained with improved WR at VU with the other members of CLEOPATRA (notably the 7S/Un. Granada people).

#3. Complete low-bandwidth PLL between improved WR and ultra-stable clean-up oscillator (DMTD + digital servo) for H-maser frequency transfer. Note that this work will also be submitted to the next-gen VLA community studies program, with the same deadline



Original WR switch



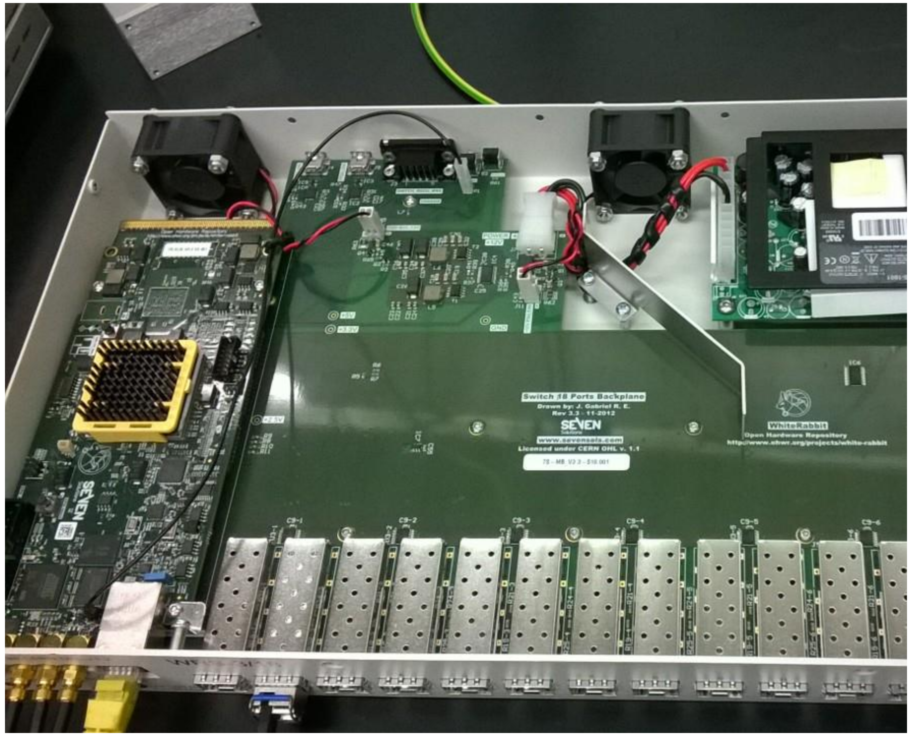


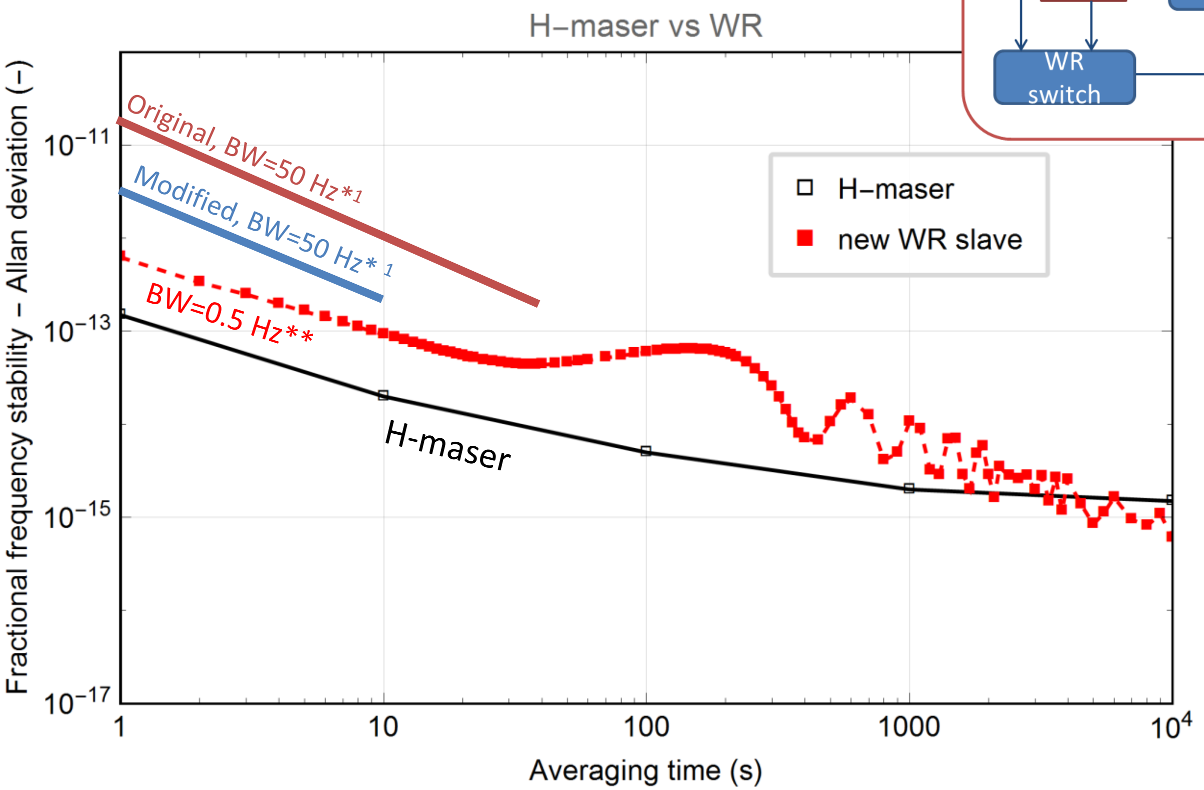
Performance of the original WR switch:

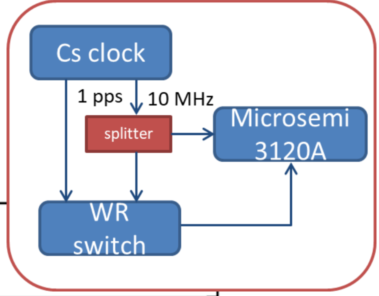
- Frequency stability of the original WR switch is not sufficient to transfer a H-maser signal without sacrificing the stability of the signal.

1 www.ohwr.org/attachments/4467/Report_WRS_MR_rev02.pdf

Modified WR switch V1







Modifications:

- At Grand Master side, softPLL is bypassed by external reference. [1]
- At Slave side, softPLL values are optimized. [1]

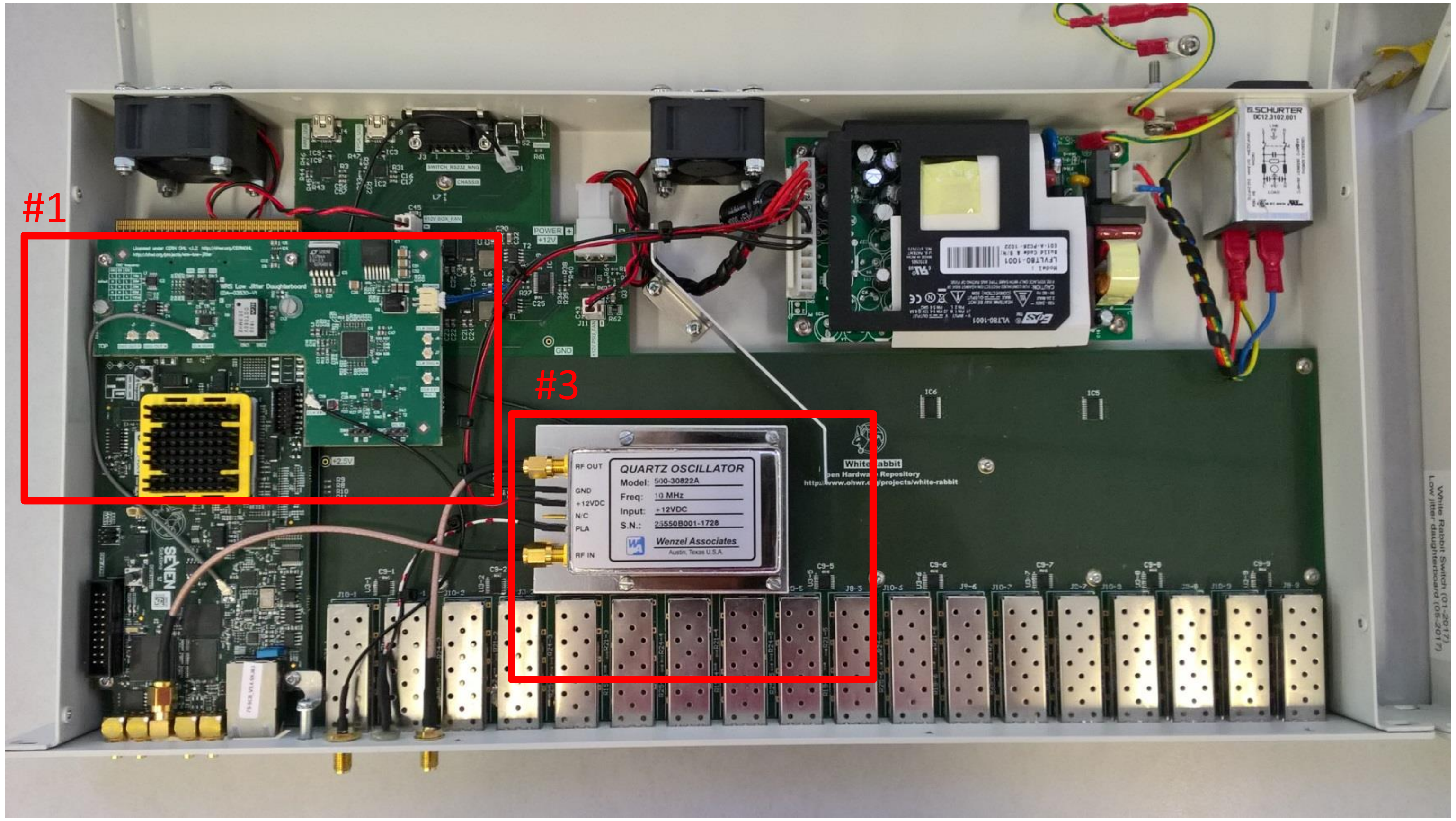
Performance:

- Frequency stability is increased one order of magnitude at 1 s.
- The Long term measurement (BW=0.5 Hz) shows oscillations in the Allan deviation. This indicates the temperature sensitivity of the main PCB board. The measurement is performed in a room with temperature fluctuations of ± 0.5 degrees Celsius over a period of 400 s. The clock shaper on the main PCB board turns out to be sensitive to temperature fluctuations, because it is designed with a single ended input.

*bandwidth (BW) of microsemi 3120A is set to 50 Hz
**BW of microsemi 3120A is set to 0.5 Hz. This affects the level of the Allan deviation curve. A bandwidth of 0.5 Hz is used for long term measurements to decrease the amount of data. This immidiately shows what a clean-up oscillator with a phase lock bandwidth of ~0.5 Hz would do.

1 www.ohwr.org/attachments/4467/Report_WRS_MR_rev02.pdf

Modified WR switch V2



Two modified WR switches are built:

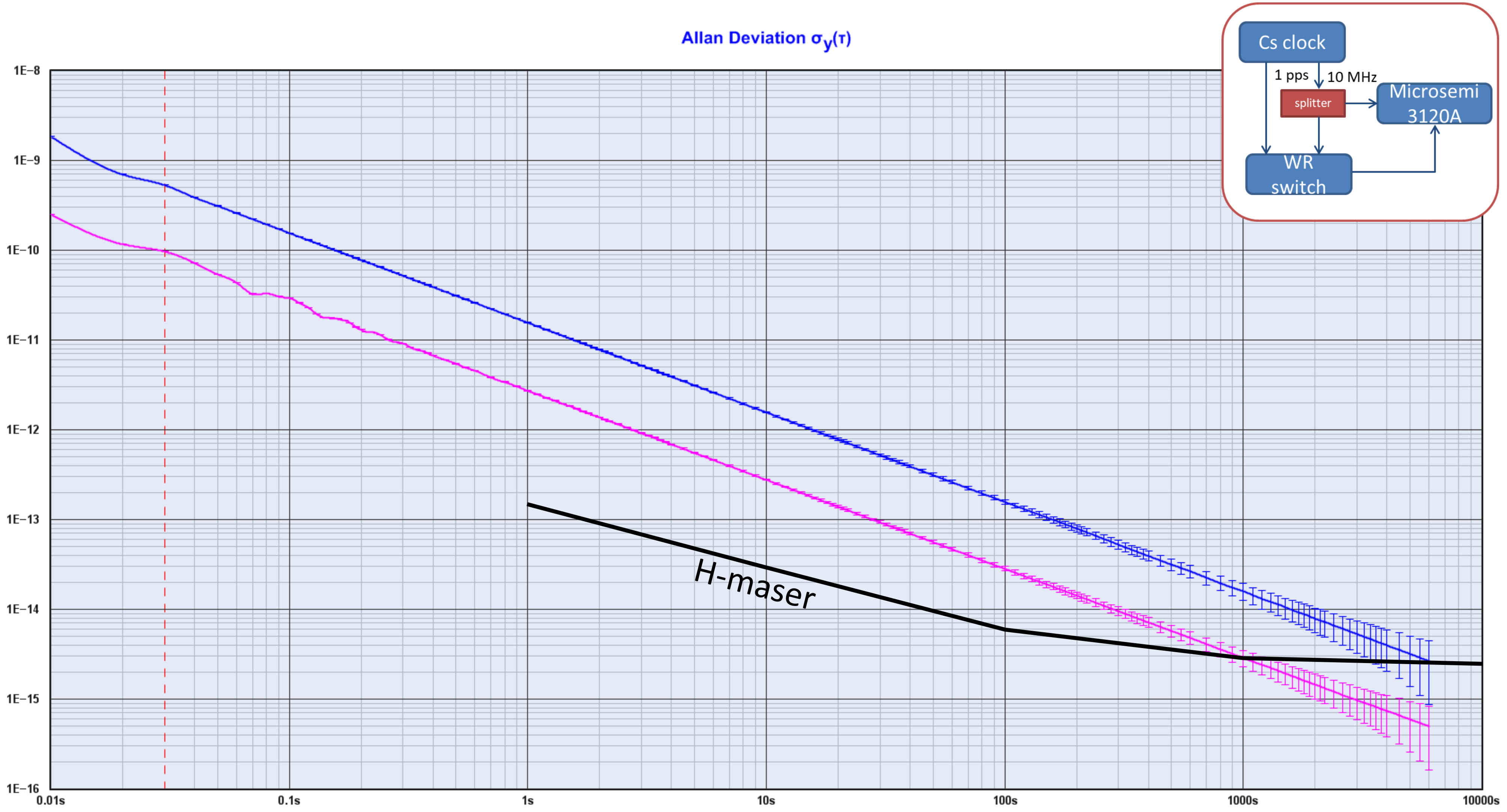
1. With LJD and PLO with BW of 0.1 Hz
2. With LJD and PLO with BW of 1 Hz

Modifications (deliverables):

- #1: Low Jitter Daughter board[2] (LJD) added **to decrease temperature sensitivity** and increase frequency stability. The LJD contains a low noise VCTXO and a clock shaper that is designed with differential inputs. Using the LJD, the clock shaper and VCTXO of the main PCB board are bypassed.
- #3: Phase Locked Oscillator (PLO from Wenzel) added to increase frequency stability between 1-10 s. The PLO is used to clean-up the output frequency of the slave.

2 http://www.ohwr.org/projects/wrs-low-jitter/wiki

First results – Performance LJD WR switch (without PLO) - Grand Master mode

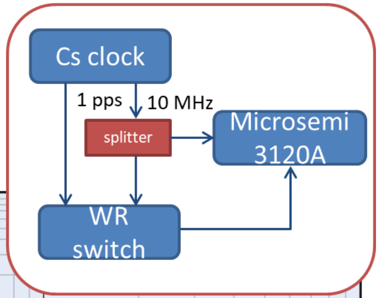


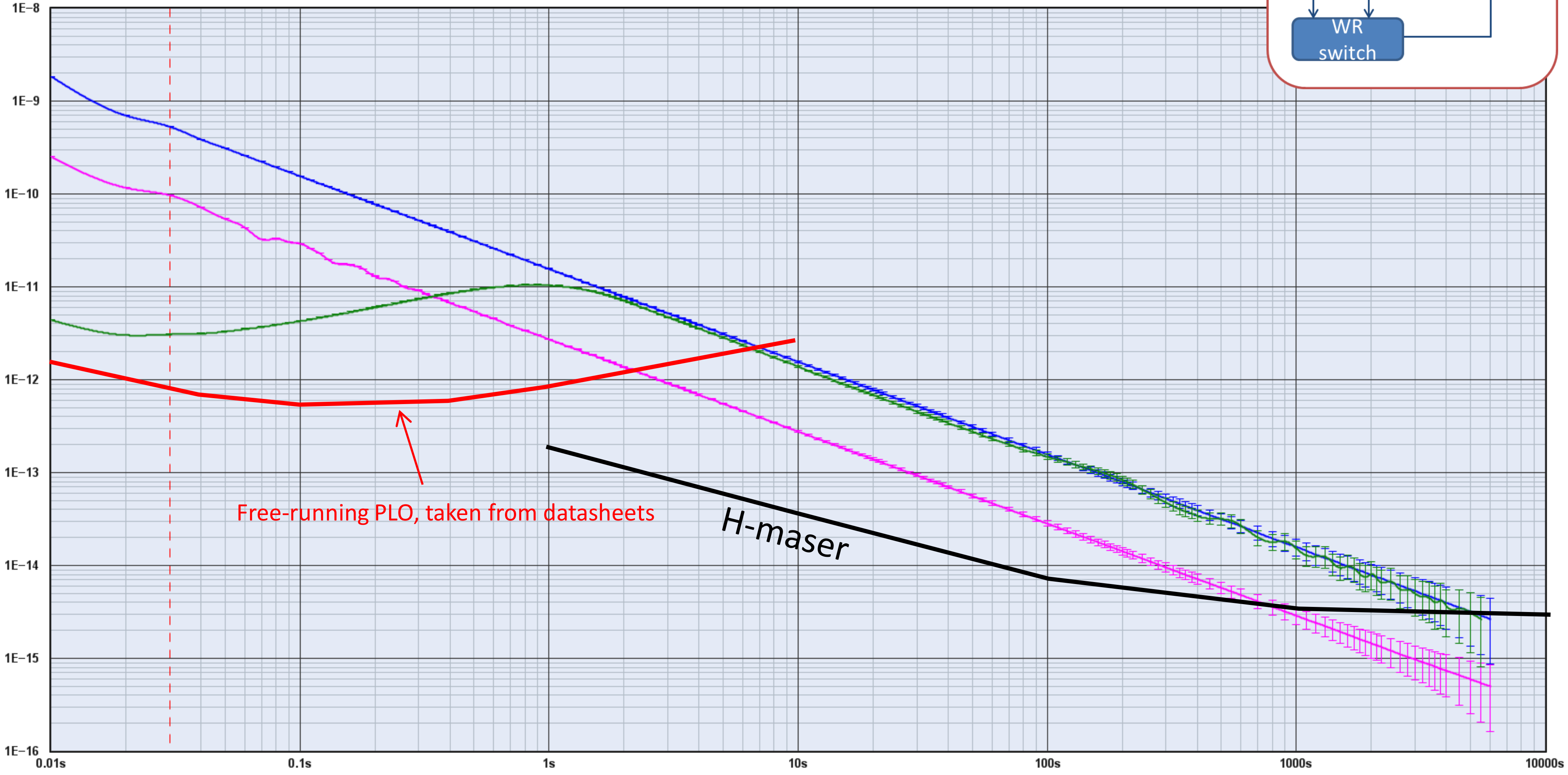
Trace	Notes	Input Freq	Sample Interval	ADEV at 0.03s	Duration	Acquired	Instrument
original WR switch - Grand master		10.000 MHz	0.010 s	5.34E−10	7h 0m 0s	2520000 pts	Symmetricom 3120A
LJD WR switch - Grand Master		10.000 MHz	0.010 s	9.75E−11	7h 0m 0s	2520000 pts	Symmetricom 3120A

Performance:

- Frequency stability of LJD WR switch - Grand Master (Blue) is ~5.5 times more stable in comparison with the original switch (purple). The temperature sensitivity is strongly suppressed (not visible in Allan deviation anymore).

First results – Performance (LJD+PLO) WR switch – Grand Master mode*





Trace	Notes	Input Freq	Sample Interval	ADEV at 0.03s	Duration	Acquired	Instrument
original WR switch - Grand master		10.000 MHz	0.010 s	5.34E−10	7h 0m 0s	2520000 pts	Symmetricom 3120A
LJD WR switch - Grand Master		10.000 MHz	0.010 s	9.75E−11	7h 0m 0s	2520000 pts	Symmetricom 3120A
(LJD+PLO 0.1 Hz) WR Switch - Grand Master		10.000 MHz	0.010 s	3.12E−12	6h 13m 19s	2239858 pts	Symmetricom 3120A

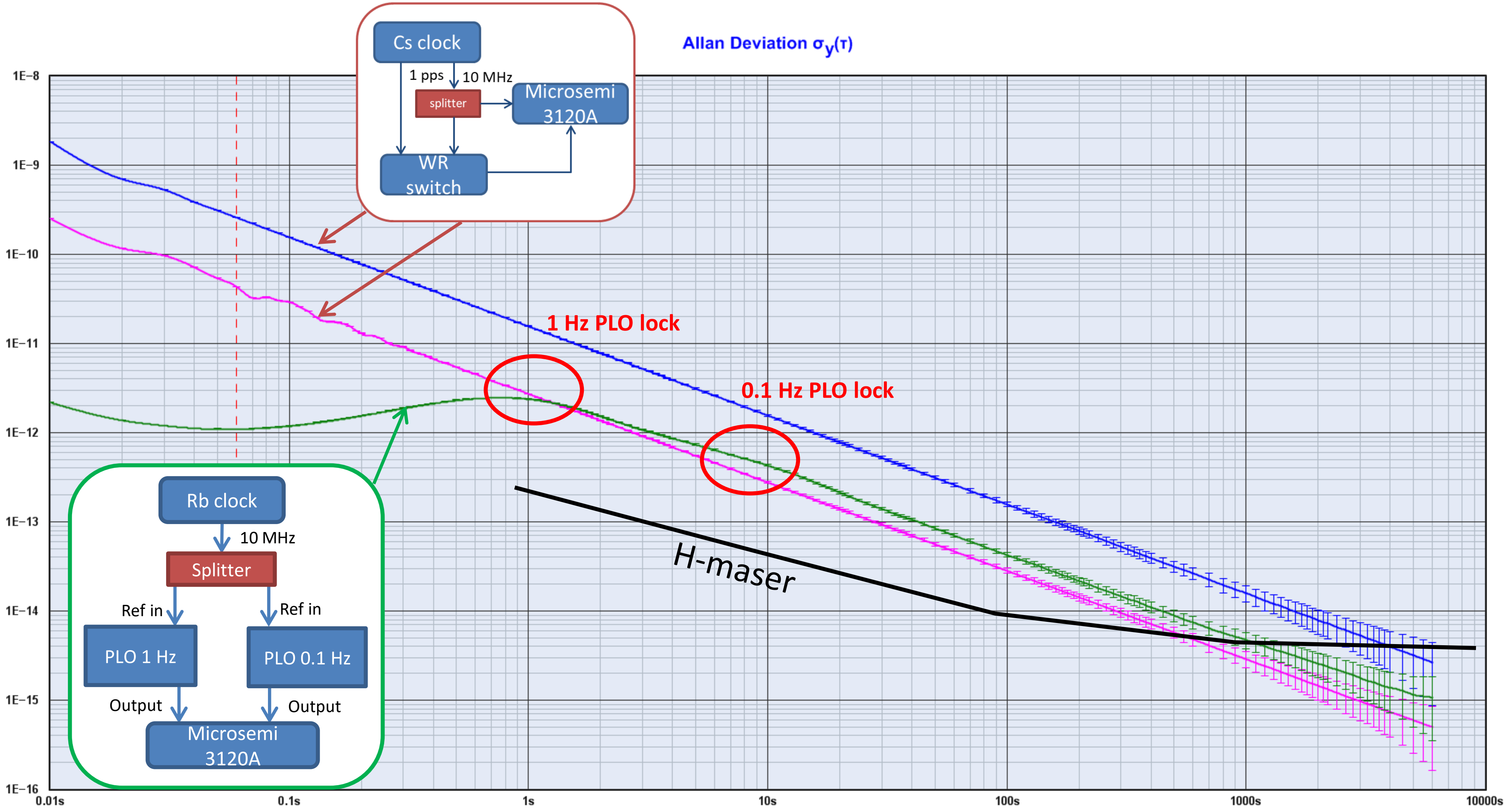
Performance:

- Frequency stability of the (LJD+PLO) WR switch - Grand Master (Green) is similar to that of the original WR switch for averaging times > 1 s. Moreover, the frequency stability between 0.01 s and 1 s is worse than expected (Red), since the PLO is free-running between these averaging times.

  All this unexpected extra noise turns out to be caused by our reference, the Cesium clock!

*The PLO will normally only be used at boundary clocks.

First results – Performance (LJD+PLO) WR switch



Trace	Notes	Input Freq	Sample Interval	ADEV at 0.06s	Duration	Acquired	Instrument
original WR switch - Grand master		10.000 MHz	0.010 s	2.60E−10	7h 0m 0s	2520000 pts	Symmetricom 3120A
LJD WR switch - Grand Master		10.000 MHz	0.010 s	4.34E−11	7h 0m 0s	2520000 pts	Symmetricom 3120A
PLO 0.1 Hz v PLO 1 Hz, both locked to Rubidium		10.000 MHz	0.010 s	1.11E−12	7h 0m 0s	2520000 pts	Symmetricom 3120A

Performance:

- To indicate the performance of the (LJD+PLO) WR switch, we compared two PLOs with each other, which are both locked to a Rubidium clock (Green). Note that the Allan deviation now contains noise from both PLOs.

- **A better reference (H-maser) is needed to measure the real performance of the (LJD+PLO) WR switch. With a better reference we could also determine which PLO is more suited for this application (1 Hz or 0.1 Hz BW).**

Conclusion and Outlook

- The frequency stability of the LJD WR switch - Grand Master is ~5.5 times more stable in comparison with the original WR switch.
- In comparison with the original WR Switch, the temperature sensitivity of the LJD WR switch is strongly suppressed.

- The implementation of the PLO at the slave switch will increase the frequency stability by ~3 orders of magnitude at 0.01 s averaging time and by ~2 orders of magnitude at 0.1 s averaging time.

- **A better frequency reference is needed to measure the real performance of the (LJD+PLO) WR switch.**